

1           1.    A method comprising:  
2                forming a first trench on a semiconductor  
3 structure;  
4                covering said first trench and said structure;  
5                etching said covering while leaving a portion of  
6 said covering in said first trench; and  
7                forming a second trench across said first trench  
8 shallower than the first trench.

1           2.    The method of claim 1 including forming two  
2 trenches of different depths using only one polishing step.

1           3.    The method of claim 2 including polishing both  
2 trenches together in the same step after both trenches have  
3 been formed.

1           4.    The method of claim 1 wherein covering one of  
2 said trenches includes covering said trench with a spin on  
3 glass.

1           5.    An integrated circuit comprising:  
2                a semiconductor structure;  
3                a first trench formed of a first depth in said  
4 semiconductor structure; and  
5                a second trench formed of a second depth crossing  
6 said first trench, deeper than said first depth, in said

7 semiconductor structure and said second trench housing said  
8 second depth where said second trench crosses said first  
9 trench.

1           6.    A method comprising:  
2                   forming a first trench in a semiconductor  
3 structure;  
4                   forming a covering for the first trench and said  
5 structure to prevent further trench etching of said first  
6 trench;  
7                   etching through said covering on the structure  
8 while leaving a portion of said covering in said first  
9 trench; and  
10                  with said first trench covered, trench etching a  
11 second trench that is shallower than said first trench.

1           7.    The method of claim 6 wherein covering said first  
2 trench includes covering said first trench with spin on  
3 glass.

1           8.    The method of claim 6 including forming a  
2 covering that is deeper in said first trench than over the  
3 structure.

1           9.    The method of claim 6 including covering said  
2 first trench with a spin-on glass.

1           10. An integrated circuit comprising:  
2               a semiconductor structure;  
3               a first trench formed of a first depth in said  
4 semiconductor structure;  
5               a covering on said first trench and over said  
6 semiconductor structure, said covering being thicker in  
7 said first trench than over said semiconductor structure;  
8 and  
9               said covering having an opening to define a  
10 region for a second trench.

1           11. The circuit of claim 10 wherein said covering is  
2 spin-on glass.

1           12. A method comprising:  
2               forming a first trench and then a second trench  
3 wherein said first trench is deeper than said second  
4 trench; and  
5               covering said deeper trench while forming said  
6 shallower trench.

1           13. The method of claim 12 including forming said  
2 covering thicker in said deeper trench than over said  
3 structure.

1           14. The method of claim 13 including covering said  
2 deeper trench in said structure with spin-on glass.

1           15. The method of claim 13 including defining an  
2 opening on said structure through said covering and etching  
3 said shallower trench.